Scalable Room Temperature Control Electronics for Advanced High-Fidelity Qubit Control

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***Abstract*— Quantum bit control systems using room temperature electronics provide universities and research institutions a cost-effective entry into quantum computing. Various approaches address the need for straightforward qubit controllers, particularly those based on AMD's next-generation RFSoC FPGA, which integrate adaptive SoCs with internal ADCs and DACs. As superconducting qubit architectures advance to incorporate flux elements for direct Z axis control and the number of qubits grows, the demand for high-quality and numerous control channels increases. This paper explores the requirements for integrating and expanding the QiController electronics from Karlsruhe Institute of Technology. The new system includes up to ten cards capable of driving a total of 240 direct flux lines. Our joint system design leverages the modularity, scalability, and thermal management of the industrial Standard ATCA, ensuring robust performance and ease of maintenance in this multi-FPGA setup. Initial unit tests of the electronics show improvements in noise levels and quality, suggesting that future verification on real qubit devices could establish this approach as a viable solution for scalable room-temperature control hardware.**

Keywords—QSolid, Qubit control, Open Quantum Hardware, Quantum computing, Flux Control, FPGA, ATCA, PICMG

I. Introduction

In quantum computing, experimentalists and engineers are searching for the optimal qubit materials, studying various solutions such as superconducting qubits, trapped ions, and semiconducting- or spin qubits. For small-scale QPU demonstrators and technology investigations, commercial QC control systems have become the gold standard in reputable laboratories and universities, offering flexible commissioning with reduced complexity and brute force scalability. These specialized metrology companies like Zurich Instruments, Quantum Machines, Qblox, Keysight offer application-specific all-in-one solutions with robust specifications, capable of handling hundreds or even thousands of qubits.

Notably, commercial high-performance computing (HPC) offered by Google, IBM, Intel, Microsoft, and Amazon AWS, are developing custom room-temperature qubit control electronics tailored to meet their specific system integration demands, providing optimal computing solutions for their qubit devices and customers [1].

Smaller research groups focusing on qubit control technology seek full access to the entire electronics stack, while other academic laboratories require affordable platforms for student use. Platforms with the newest AMD Xilinx RFSoC generation FPGA SoC are adapted to readout and drive tens of qubits based on reasonable ready-to-use evaluation boards and customized front ends. Solutions such as *QICK* from Fermi Lab, *QubiC* from Berkeley and *QiController* by the Karlsruhe Institute of Technology (KIT) [2, 3] became a suitable way to provide qubit control electronics to their students and research groups under open quantum hardware (OQH) encompassing open source software and toolkits [4]. Within the BMBF-funded project QSolid - Quantum Computer in the Solid State, a quantum computer demonstrator based on cutting-edge technology from Germany will be developed using superconducting circuits, featuring processor generations with varying performance profiles focused on size, precision, and application relevance.

The desired coupled ladder architecture of the qubit device leads to a significant imbalance between the X/Y-axis control, readout lines and the explicit Flux-DAC outputs. These direct RF lines for Z-axis manipulation are a limitation of OQH platforms offering a maximum of 16 RFSoC internal DACs. This limit applies unless they are extended with external electronics.

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II. System Implementation

For the final project goal of realizing a quantum computer with 30 qubits, the RFSoC System on Modules (SoM) and additional external DAC devices need to be combined in power, clock and interface domains. Since performant room temperature components and convenient SoM of the utilized RFSoCs exist, a new architecture taking advantage of the industrial standard AdvancedTCA, specified under PICMG 3.0 has been chosen [3].

The system architecture comprises two different slot cards in *ATCA* specific design: the *Hub* and the *Node* card. Both boards fully support the ATCA backend and specifications of the chosen Dual Dual Star crate by nVent, Schroff with a safety cooling capacity of 450 Watt per slot [3].

A. The Hub Card

The *Hub* represents the integrated version of the proven QiController capabilities shown in Fig. *1*. The design consists of the iW Rainbow G42M SoM from iWave with providing an AMD ZU49DR RFSoC. Additional signal conditioning filters and BALUNs connected to the internal ADCs and DACs of the ZU49DR allow software defined qubit readout and control to the required center frequency between 4-7 GHz and a channel spacing of 50 MHz. One *Hub* controls up to 10 interconnected FPGAs through the backplane of the ATCA crate. The resulting high demand for pins of board to board connectors is met by the iW Rainbow G42M SoM.

B. The Node Card

The *Node* is subject of the first midterm milestone as it extends the existing platform QiController with the required Flux DAC lines. The PCB holds three units with single AMD Kintex Ultrascale XCKU115 FPGA driving eight LTC2000 from Analog Devices each. These 2.5 GS/s current steering DACs meet the demand on the firing synchronization of 50 ps. This low latency approach uses up all 598 HP I/O pins of the driving XCKU115 FPGA since one LTC2000 requires 35 LVDS pairs for parallel waveform data reception [5].

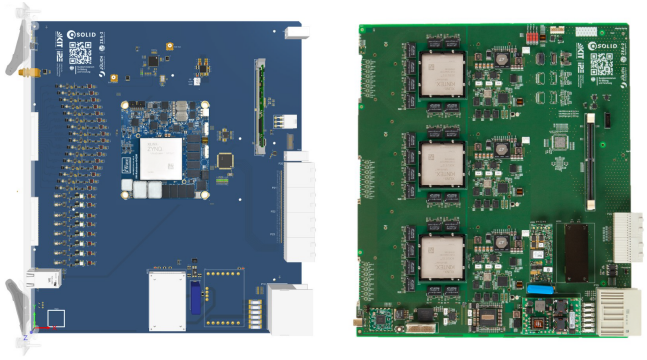

Fig. 1. The *Hub* card (illustration, left) consists of the iW Rainbow G42M SoM, iWave Systems with an AMD ZU49DR RFSoC, The *Node* (right) combines three AMD Kintex Ultrascale XCKU115 with eight LTC2000 DACs each.

The analog current outputs of the LTC2000 DAC provide up to ±40 mA to a differential impedance with a noise spectral density of -156 dBm/Hz [5]. The filter specific notches in stopband are used to suppress the digital DAC frequencies from the output signal. The required flux signal output from DC to 1 GHz @ 10dBm for pre-shaping is then filtered through a discrete 5th order inverted Chebyshev to a cutoff frequency of 500 MHz with a group delay of 0.8 ns (Fig. *2*).

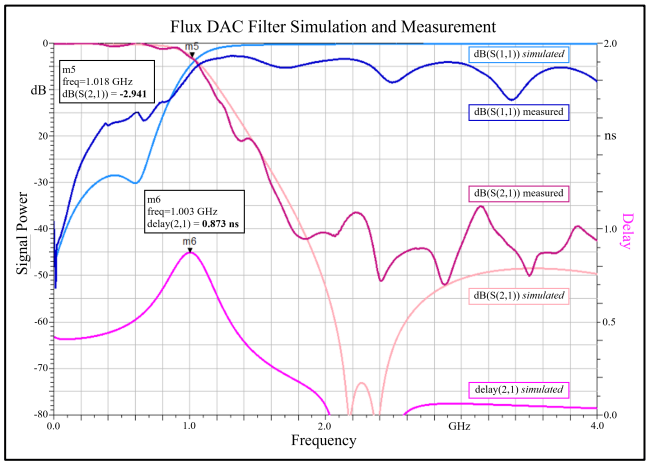

Fig. 2. Flux DAC discrete output filter simulated with ADS, Keysight compared with measured data from vector network analyzer E5071C, Keysight.

III. Interfaces

The *QiController* based system is integrated into an HPC environment via Python client qiclib and accessible through commonly used Jupyter(lab) notebooks utilizing the high-level language called QiCode [6]. The proposed architecture ensures the interconnectivity of the FPGA domains via established bridging implementations through the backplane using the AMDs Chip2Chip IP core [7].

With a fully stocked crate, the differential flux lines scale to a total of 480 quasi-differential coaxial cables. Using Rosenberger's 16 channel *WSMP* block plug edge mount connector, with a return loss of 25 dB (DC to 12 GHz), ensures a modular cable composition [8].

IV. Conclusion

The architecture chosen promises a scalable approach for the extension with flux lines of an established OQH *QiController* from KIT. Verifications on a cold qubit device installed at a cryo-lab from Forschungszentrum Juelich GmbH have proven the ability to control qubits, run common qubit gates and complex circuits. The development of a qubit control demonstrator for a 30 qubit device offers valuable insights into transitioning from room-temperature to cryogenic electronics, highlighting a critical pathway for future advancements in scalable quantum computing hardware.

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